Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] What is claimed is:

1. A pre-charge and sense out circuit of a differential type ROM for sensing logic data stored in a memory cell of the ROM, the memory cell being capable of connecting to one of a first bit line and a second bit line for providing digital signals to the first bit line or the second bit line, the pre-charge and sense out circuit comprising:
a pre-charge module electrically connected to the first and the second bit lines for pre-charging the first and the second bit lines;
a selecting module electrically connected to the first bit line, the second bit line, a first data line, and a second data line, for transmitting signals on the first bit line to the first data line and signals on the second bit line to the second data line according to a first control signal;
a charge sharing module electrically connected to the first and the second data lines for pre-charging the first and the second data lines, and for sharing electrical charges stored in the charge sharing module with the first and the second data lines according to a second control signal; and
a sensing module electrically connected to the first and

the second data lines for sensing signals on the first and the second data lines to generate an output signal.

[c2] 2.The pre-charge and sense out circuit of claim 1 wherein the charge sharing module comprises:

a first capacitor whereof one end is electrically connected to a first node and another end is grounded, for storing electrical charges to be shared with the first data line;

a first PMOS transistor whereof a source is electrically connected to a power supply voltage, a gate is electrically connected to the second control signal, and a drain is electrically connected to the first node;

a first NMOS transistor whereof a drain is electrically connected to the first node, a gate is electrically connected to the second control signal, and a source is electrically connected to the first data line;

a second capacitor whereof one end is electrically connected to a second node and another end is grounded, for storing electrical charges to be shared with the second data line;

a second PMOS transistor whereof a source is electrically connected to the power supply voltage, a gate is electrically connected to the second control signal, and a drain is electrically connected to the second node; and

a second NMOS transistor whereof a drain is electrically

connected to the second node, a gate is electrically connected to the second control signal, and a source is electrically connected to the second data line.

[c3] 3.The pre-charge and sense out circuit of claim 2 wherein the charge sharing module further comprises:
a third NMOS transistor whereof a drain is electrically connected to the first data line, a gate is electrically connected to a complementary signal of the second control signal, and a source is grounded, for pre-charging the first data line; and
a fourth NMOS transistor whereof a drain is electrically connected to the second data line, a gate is electrically connected to the complementary signal of the second control signal, and a source is grounded, for pre-charging the second data line.

[c4] 4.The pre-charge and sense out circuit of claim 1 wherein the pre-charge module comprises:
a first charging NMOS transistor whereof a drain is electrically connected to the first bit line, a gate is electrically connected to a complementary signal of the first control signal, and a source is grounded; and
a second charging NMOS transistor whereof a drain is electrically connected to the second bit line, a gate is electrically connected to the complementary signal of the first control signal, and a source is grounded.

[c5] 5.The pre-charge and sense out circuit of claim 1 wherein the selecting module comprises:
a first selecting NMOS transistor whereof a drain is electrically connected to the first bit line, a gate is electrically connected to the first control signal, and a source is electrically connected to the first data line; and
a second selecting NMOS transistor whereof a drain is electrically connected to the second bit line, a gate is electrically connected to the first control signal, and a source is electrically connected to the second data line.

[c6] 6.The pre-charge and sense out circuit of claim 1 wherein the sensing module comprises:
a first isolating NMOS transistor whereof a drain is electrically connected to the first data line, a gate is electrically connected to a third control signal, and a source is electrically connected to a first output signal line;
a second isolating NMOS transistor whereof a drain is electrically connected to the second data line, a gate is electrically connected to the third control signal, and a source is electrically connected to a second output signal line;
a first inverter whereof an input end is electrically connected to the second output signal line and an output end is electrically connected to the first output signal line; and

a second inverter whereof an input end is electrically connected to the first output signal line and an output end is electrically connected to the second output signal line;

wherein the output signal is generated on the first output signal line, and a complementary signal of the output signal is generated on the second output signal line.

[c7] 7.The pre-charge and sense out circuit of claim 6 wherein the sensing module further comprises an enabling PMOS transistor whereof a source is electrically connected to a power supply voltage, a gate is electrically connected to a fourth control signal, and a drain is electrically connected to the first and the second inverter, for enabling/disabling the sensing module according to the fourth control signal.

[c8] 8.The pre-charge and sense out circuit of claim 7 wherein the first inverter comprises a PMOS transistor and an NMOS transistor, gates of the PMOS transistor and the NMOS transistor being connected to each other as the input end of the first inverter, drains of the PMOS transistor and the NMOS transistor being connected to each other as the output end of the first inverter, a source of the PMOS transistor being electrically connected to a drain of the enabling PMOS transistor, a source of the NMOS transistor being grounded.

[c9] 9.The pre-charge and sense out circuit of claim 7 wherein the second inverter comprises a PMOS transistor and an NMOS transistor, gates of the PMOS transistor and the NMOS transistor being connected to each other as the input end of the second inverter, drains of the PMOS transistor and the NMOS transistor being connected to each other as the output end of the second inverter, a source of the PMOS transistor being electrically connected to a drain of the enabling PMOS transistor, a source of the NMOS transistor being grounded.

[c10] 10.The pre-charge and sense out circuit of claim 6 wherein the sensing module further comprises:
a third NMOS transistor whereof a drain is electrically connected to the first output signal line, a gate is electrically connected to a fifth control signal, and a source is grounded, for pre-charging the first output signal line; and
a fourth NMOS transistor whereof a drain is electrically connected to the second output signal line, a gate is electrically connected to the fifth control signal, and a source is grounded, for pre-charging the second output signal line.